The AHA4501 is a single-chip Forward Error Correction LSI device using Turbo Product Codes (TPC). The device operates as a block code encoder at the input or a block code decoder at the output of a communication channel. Figure 1 shows a functional block diagram of the device. Turbo Product Codes offer a higher performance alternative to Reed-Solomon or Reed-Solomon concatenated with Viterbi error correction methods.

When encoding, a block of data is input into the device’s internal RAM. The device then calculates error correction (ECC) and parity bits across each dimension of the block, appends the ECC and parity bits to the block, and then outputs the encoded block.

When decoding, the device accepts soft decision values and stores the data as a block in its internal RAM. The block is then decoded iteratively by running the block through the device’s soft in/soft out (SISO) decoder. The device iterates a block to the maximum programmed iteration limit. The decoded block is then output through the device output data port.

Configuration, control and status of the device is accomplished through read/writable registers via a standard microprocessor interface. The device also has an interrupt output signal.

**FEATURES**

**PERFORMANCE:**
- Maximum 50 Mbits/second data rate encoding and up to 36 Mbits/second data rate decoding with a 50 MHz clock
- Two or more devices can be used in parallel to increase throughput
- Optional “helical” interleaving (encoding) and deinterleaving (decoding)

**FLEXIBILITY:**
- Internal buffering allows continuous data streaming
- Programmable block size from 256 to 4096 bits
- Two or three dimensional blocks
- Programmable number of iterations per block up to 32
- Programmable quantization up to 6-bits for soft or hard decision input data (decoding)
- Support for external synchronization

**SYSTEM INTERFACE:**
- Serial or 8-bit parallel input and output data ports
- Selectable microprocessor interface for Intel or Motorola processors
- Control Commands for: Decode, Encode, Soft Reset, Resynchronize and Dump Current Block
- System Interrupts include Block Decode Complete, Block Correction Incomplete, Sync Mark Mismatch
- Number of corrections per block accumulated in an internal register

**OTHERS:**
- 3.3 Volt operation
- 100 pin quad flat package
- Output signals may be tristated to facilitate board level testing
- Commercial or industrial temperature rating

**APPLICATIONS**

Various communication systems including, but not limited to:
- Wireless
- Satellite
- Networking

This product is covered under multiple patents held or licensed by Comtech EF Data Corp.
This product is covered by a Turbo Code Patent License from France Telecom - TDF - Groupe des ecoles des telecommunications.

*Request the AHA4501 Product Specification for complete details
**FUNCTIONAL OVERVIEW**

**ERROR CORRECTION CAPABILITY**

The AHA4501 provides various levels of error correction based on programmable parameters including block size, iterations executed on each block and the number of quantization bits. Higher numbers of iterations provide greater error correction capability at the expense of lower data throughput.

AHA4501 block sizes range from 256 to 4096 bits and can be configured as a 2D or 3D array. The device also supports several block types within each block size, each with different code rates. Throughput latency depends on the block size.

Table 1 gives a partial list of the code types supported, including overall code block size and data size in bits. Since Turbo Product Codes are block codes, they can be shortened to achieve virtually any block size and rate below those shown in the table. Shortening of the codes must be done in external hardware.

The number of input quantization bits can be varied from 1 to 6 bits when decoding. More quantization bits provide better error correction capability at the expense of greater complexity in the system front end.

**ENCODING**

When encoding, data is input either serially or in 8-bit parallel using a fully synchronous ready/accept handshake protocol. Data input to the device is stored in the Original Array (OA) SRAM as either a 2D block consisting of \(k_1 \times k_2\) bits or a 3D block consisting of \(k_1 \times k_2 \times k_3\) bits. Each dimension length of a block can be different and can range from 4 to 64 bits.

After an entire block is loaded, the device calculates a number of ECC bits and one parity bit for each of the rows and columns of the block and appends them to their respective rows and columns. This brings the total number of bits in a 2D block to \(n_1 \times n_2\). For example, a 2D block built from \(k_1 \times k_2\) input bits is modified into a block of \(n_1 \times n_2\) bits. The common notation for such a block is \((n_1, k_1) \times (n_2, k_2)\).

The encoded block is then output from the Hard Decision Array (HDA) SRAM serially on ODATA[0].

**DECODING**

When decoding, the device accepts 1 to 6 bit quantization soft values from an A to D converter and stores the values in OA SRAM as either a 2D block consisting of \(n_1 \times n_2\) values or as a 3D block consisting of \(n_1 \times n_2 \times n_3\) values.

Decoding is done by iteratively passing a block through the SISO decoder a number of times until there are no errors to correct or until a predetermined number of iterations has been completed. One iteration of a block requires that all \(n_1\) and \(n_2\) axes (2D) or all \(n_1, n_2\), and \(n_3\) axes (3D) be passed through the SISO decoder. Intermediate data generated by each iteration is stored in the Intermediate Storage Array (ISA) SRAM.

When the device has completed iterating, the block is output from the HDA SRAM either serially on ODATA[0] or in parallel on ODATA[7:0] using a fully synchronous ready/accept handshake protocol.

The decoder data rate is dependent on the code type and the number of iterations. Table 2 gives approximate data rates at different iterations. Note that multiple devices may be run in parallel with minimal external logic to achieve higher data rates.
Table 1: Code Types Supported by AHA4501

<table>
<thead>
<tr>
<th>BLOCK SIZE (bits)</th>
<th>DATA SIZE (bits)</th>
<th>RATE</th>
<th>CODE STRUCTURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>4096</td>
<td>3249</td>
<td>0.793</td>
<td>2D</td>
</tr>
<tr>
<td>4096</td>
<td>2028</td>
<td>0.495</td>
<td>3D</td>
</tr>
<tr>
<td>4096</td>
<td>1331</td>
<td>0.325</td>
<td>3D</td>
</tr>
<tr>
<td>2048</td>
<td>1482</td>
<td>0.724</td>
<td>2D</td>
</tr>
<tr>
<td>2048</td>
<td>858</td>
<td>0.419</td>
<td>3D</td>
</tr>
<tr>
<td>1024</td>
<td>676</td>
<td>0.660</td>
<td>2D</td>
</tr>
<tr>
<td>1024</td>
<td>363</td>
<td>0.354</td>
<td>3D</td>
</tr>
<tr>
<td>512</td>
<td>286</td>
<td>0.559</td>
<td>2D</td>
</tr>
<tr>
<td>256</td>
<td>121</td>
<td>0.473</td>
<td>2D</td>
</tr>
</tbody>
</table>

Table 2: Data Rates* at Different Iterations

<table>
<thead>
<tr>
<th>ITERATIONS</th>
<th>DATA RATE (Mbits/sec)**</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>36 25 18</td>
</tr>
<tr>
<td>3</td>
<td>25 18 14</td>
</tr>
<tr>
<td>4</td>
<td>19 9 4.9</td>
</tr>
<tr>
<td>6</td>
<td>7 4.9 1.9</td>
</tr>
<tr>
<td>12</td>
<td>2.7 1.9 1.1</td>
</tr>
<tr>
<td>32</td>
<td>2.7 1.9 1.1</td>
</tr>
</tbody>
</table>

* Reflects coded rate which includes error correction bits.
** Max rate for fastest codes.

Figure 2: Turbo Product Code vs. Reed-Solomon/Viterbi Performance Comparison

(64,57) x (64,57) Hamming Product Code, Rate = 0.793

Figure 3: Comparison of TPC Code Types

Hamming Product Code, Block Size 4096 bits

Uncoded PSK Channel
(64,57)x(64,57), rate=.793
(32,26)x(32,26)x(4,3), rate=.495
(16,11)x(16,11)x(16,11), rate=.325
PERFORMANCE CURVES

Figure 2 shows a comparison between the error correction performance of the AHA4501 TPC and the concatenated Reed-Solomon/Viterbi compared with uncoded Phase Shift Keying assuming a channel with additive white Gaussian noise (AWGN). Note that the TPC implementation consistently outperforms RS/Viterbi using only two iterations. Additional iterations increase performance.

Figure 3 compares different block codes each with a 4096 bit block size. Note that error correction performance is increased by using block codes with lower code rates.

Figure 4: Performance Curve for (64,56) x (64,57), rate = 0.793 Code

Figure 4 shows the $E_b/N_0$ required to achieve a Bit Error Rate (BER) of $10^{-5}$ with various numbers of iterations and input quantization bits. Note that a very low $E_b/N_0$ ratio can be obtained using only 3 bits of quantization and 3 or 4 iterations per block.

ABOUT AHA

The AHA Products Group (AHA) of Comtech EF Data Corporation develops and markets superior integrated circuits, boards, and intellectual property cores for improving the efficiency of communications systems everywhere. AHA has been setting the standard in Forward Error Correction and Lossless Data Compression for many years and provides flexible and cost effective solutions for today’s growing bandwidth and reliability challenges. Comtech EF Data is a wholly owned subsidiary of Comtech Telecommunications Corporation (NASDAQ™ CMTL). For more information, visit: www.aha.com.

ORDERING INFORMATION

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<th>PART NUMBER</th>
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<tr>
<td>AHA4501A-050 PQC</td>
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</tr>
<tr>
<td>AHA4501A-050 PQI</td>
<td>36 Mbits/sec Turbo Product Code Encoder/Decoder - Industrial Temperature</td>
</tr>
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